AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

Listing of Claims:

Claim 1 (Currently Amended): A semiconductor memory device comprising:

a first memory cell having a first gate electrode, a first diffusion layer and a second diffusion layer, the first and second diffusion layers arranged in a semiconductor substrate to be adjacent to the first gate electrode;

a first contact layer connected to the first diffusion layer of the first memory cell;

a second contact layer connected to the first contact layer;

a first bit line connected to the second contact layer and arranged above the first gate electrode of the first memory cell;

a second memory cell having a second gate electrode, a third diffusion layer and a fourth diffusion layer, the third and fourth diffusion layers arranged in a semiconductor substrate to be adjacent to the second gate electrode, the second gate electrode of the second memory cell electrically connected to the first gate electrode of the first memory cell, the first and second memory cells arranged in a direction perpendicular to the first bit line;

a third contact layer connected to the third diffusion layer of the second memory cell;

a fourth contact layer connected to the third contact layer;

a second bit line connected to the fourth contact ~~third diffusion~~ layer, arranged above the second gate electrode of the second memory cell, and arranged parallel to the first bit line;

an element isolation insulating layer ~~region~~ formed in an upper portion of the semiconductor substrate and arranged between the first and second memory cells; and

a conductive layer commonly connected to the second diffusion layer of the first

memory cell and the fourth diffusion layer of the second memory cell, a height of the conductive layer substantially being coplanar with a height of the first contact layer, the conductive layer formed to be contact with the element isolation insulating layer ~~region~~ that is arranged between the second diffusion layer of the first memory cell and the fourth diffusion layer of the second memory cell.

Claim 2 (Previously Presented): The semiconductor memory device according to claim 1, wherein the first contact layer includes a W layer.

Claim 3 (Previously Presented): The semiconductor memory device according to claim 1, wherein the first contact layer includes a first conductive film and a second conductive film.

Claim 4 (Previously Presented): The semiconductor memory device according to claim 3, wherein the first conductive film is Ti.

Claim 5 (Previously Presented): The semiconductor memory device according to claim 3, wherein the second conductive film is W.

Claim 6 (Previously Presented): The semiconductor memory device according to claim l, wherein the semiconductor memory device is one of a NAND type nonvolatile memory device and a NOR type memory device.

Claim 7 (Original): A memory card including the semiconductor memory device recited in claim 1.

Claim 8 (Original): A card holder to which the memory card recited in claim 7 is inserted.

Claim 9 (Original): A connecting device to which the memory card recited in claim 7 is inserted.

Claim 10 (Original): The connecting device according to the claim 9, the connecting device is configured to be connected to a computer.

Claim 11 (Original): A memory card including the semiconductor memory device recited in claim 1 and a controller which controls the semiconductor memory device.

Claim 12 (Original): A card holder to which the memory card recited in claim 11 is inserted.

Claim 13 (Original): A connecting device to which the memory card recited in claim 11 is inserted.

Claim 14 (Original): The connecting device according to the claim 13, the connecting device is configured to be connected to a computer.

Claim 15 (Original): An IC card on which an IC chip that includes the semiconductor memory device recited in claim 1 is located.

Claim 16 (Currently Amended): A semiconductor memory device, comprising:

a plurality of memory cells each of which includes a gate electrode and first and second [[a]] diffusion layers;

an element isolation insulating layer formed in a semiconductor substrate and between the plurality of memory cells;

an insulating film formed above side and top surfaces of each gate electrode of the plurality of memory cells;

a first interlayer insulating layer formed between two gate electrodes adjacent to each other;

a first contact layer formed in the first interlayer insulating layer and connected to the first diffusion layer;

a second interlayer insulting layer formed on the first interlayer insulating layer;

a second contact layer formed in the second interlayer insulating layer and connected to the first contact layer;

a bit line connected to the second contact layer; and

a conductive layer connected to at least two of the second diffusion layers ~~other than the diffusion layer connected to the first contact layer~~, the conductive layer formed between the two gate electrodes adjacent to each other being arranged in a direction vertical to the bit line, a height of the conductive layer substantially being coplanar with a height of the first contact layer, wherein the height of the conductive layer is approximately uniform, and a bottom surface of the conductive layer is in contact with the at least two of the second diffusion layers and an upper surface of the element isolation insulating layer.

Claim 17 (Previously Presented): The semiconductor memory device according to claim 16, wherein the first contact layer includes a W layer.

Claim 18 (Previously Presented): The semiconductor memory device according to claim 16, wherein a position of a top surface of the insulating film formed above the gate electrode of the plurality of memory cells is coplanar with the top surface of the first interlayer insulating layer.

Claim 19 (Previously Presented): The semiconductor memory device according to claim 16, wherein a position of a top surface of the insulting film formed above the gate electrode of the plurality of memory cells is different from that of the top surface of the first interlayer insulating layer.

Claim 20 (Previously Presented): The semiconductor memory device according to claim 16, wherein the conductive layer is a source line.

Claim 21 (Previously Presented): The semiconductor memory device according to claim 16, wherein the plurality of memory cells is one of a NAND type nonvolatile memory device and a NOR type memory device.

Claim 22 (Previously Presented): A memory card including the plurality of memory cells recited in claim 16.

Claim 23 (Original): A card holder to which the memory card recited in claim 22 is inserted.

Claim 24 (Original): A connecting device to which the memory card recited in claim 22 is inserted.

Claim 25 (Original): The connecting device according to the claim 24, the connecting device is configured to be connected to a computer.

Claim 26 (Previously Presented): A memory card including the plurality of memory cells recited in claim l6 and a controller which controls the plurality of memory cells.

Claim 27 (Original): A card holder to which the memory card recited in claim 26 is inserted.

Claim 28 (Original): A connecting device to which the memory card recited in claim 26 is inserted.

Claim 29 (Original): The connecting device according to the claim 28, the connecting device is configured to be connected to a computer.

Claim 30 (Previously Presented): An IC card on which an IC chip that includes the plurality of memory cells recited in claim 26 is located.

Claim 31-46 (Canceled).